Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-15 (Canceled)

Claim 16 (Currently Amended): A method of forming a conductive path in a semiconductor device, comprising:

forming an ~~a first~~ insulating layer on a semiconductor substrate, the insulating layer having[[;]] ~~forming~~ a first conductive member and a second conductive member embedded therein spaced apart from each other, so that the second conductive member is below the first ~~on the first insulating layer; forming a second insulating layer on the first insulating layer and the~~ conductive member, and so that the first and second conductive ~~member is~~ members are covered by the ~~second~~ insulating layer;

forming an etching mask on the ~~second~~ insulating layer, the etching mask having an opening over the first conductive member;

etching the ~~second~~ insulating layer using the etching mask in a reaction chamber, wherein a reaction chamber pressure is not less than about 100 mTorr, a reaction gas ~~essentially~~ consists of CHF_3 and CO, a flow ratio of CHF_3 and CO is about 15/85, and a flow rate of the reaction gas is not less than about 300 sccm, so that the

~~second~~ insulating layer under the opening of the etching mask is removed and an etch stop occurs in the insulating layer between the first and second conductive members without exposing the second conductive member; and

filling a removed portion of the ~~second~~ insulating layer with a conductive material to form the conductive path.

Claim 17 (Previously Presented): A method of forming a conductive path according to claim 16, wherein the reaction chamber pressure is about 200 mTorr.

Claim 18 (Previously Presented): A method of forming a conductive path according to claim 16, wherein the semiconductor substrate is biased by a high-frequency power source.

Claim 19 (Previously Presented): A method of forming a conductive path according to claim 18, wherein the high-frequency power source is maintained at about 1600W.

Claim 20 (Currently Amended): A method of forming a conductive path according to claim 16, wherein the ~~second~~ insulating layer is made of silicon oxide.

Claim 21 (Previously Presented): A method of forming a conductive path according to claim 16, wherein the flow rate of CHF_3/CO is about 45/255 sccm.

Claim 22 (Currently Amended): A method of forming a conductive path in a semiconductor device, comprising:

providing a semiconductor structure including a semiconductor substrate, an insulating layer formed on the semiconductor substrate, and first and second [[a]] conductive members ~~member~~ formed in the insulating layer spaced apart from each other, so that the second conductive member is below the first conductive member;

forming an etching mask on the insulating layer, the etching mask having an opening over the first conductive member;

etching the ~~second~~ insulating layer using the etching mask in a reaction chamber, wherein a reaction chamber pressure is not less than about 100 mTorr, a reaction gas ~~essentially~~ consists of CHF_3 and CO, a flow ratio of CHF_3 and CO is about 15/85, and a flow rate of the reaction gas is not less than about 300 sccm, so that the insulating layer under the opening of the etching mask is removed to expose the first conductive member and an etch stop occurs in the insulating layer between the first and second conductive members without exposing the second conductive member; and

filling a removed portion of the insulating layer with a conductive material to form the conductive path.

Claim 23 (Previously Presented): A method of forming a conductive path according to claim 22, wherein the reaction chamber pressure is about 200 mTorr.

Claim 24 (Previously Presented): A method of forming a conductive path according to claim 22, wherein the semiconductor substrate is biased by a high-frequency power source.

Claim 25 (Previously Presented): A method of forming a conductive path according to claim 24, wherein the high-frequency power source is maintained at about 1600W.

Claim 26 (Currently Amended): A method of forming a conductive path according to claim 22, wherein the ~~second~~ insulating layer is made of silicon oxide.

Claim 27 (Previously Presented): A method of forming a conductive path according to claim 22, wherein the flow rate of CHF_3/CO is about 45/255 sccm.

Claim 28 (New): A method of forming a conductive path according to claim 16, wherein the opening in the etching mask is formed as misaligned laterally with respect to the first conductive member by less than 0.1 um.

Claim 29 (New): A method of forming a conductive path according to claim 16, wherein the reaction chamber pressure is 200 mTorr, the flow ratio of CHF_3 and CO is 15/85, the flow rate of the reaction gas is 300 sccm, and the opening in the etching mask is formed as misaligned laterally with respect to the first conductive member by less than

0.1 um.

Claim 30 (New): A method of forming a conductive path according to claim 29, wherein a distance between an upper surface of the first conductive member to the second conductive member is greater than 300 nm, and a hole formed during said etching has a depth from the upper surface of the first conductive member to a bottom of the hole that does not exceed 200 nm.

Claim 31 (New): A method of forming a conductive path according to claim 22, wherein the opening in the etching mask is formed as misaligned laterally with respect to the first conductive member by less than 0.1 um.

Claim 32 (New): A method of forming a conductive path according to claim 22, wherein the reaction chamber pressure is 200 mTorr, the flow ratio of CHF_3 and CO is 15/85, the flow rate of the reaction gas is 300 sccm, and the opening in the etching mask is formed as misaligned laterally with respect to the first conductive member by less than 0.1 um.

Claim 33 (New): A method of forming a conductive path according to claim 32, wherein a distance between an upper surface of the first conductive member to the second conductive member is greater than 300 nm, and a hole formed during said etching has

a depth from the upper surface of the first conductive member to a bottom of the hole that does not exceed 200 nm.